REMARKS

In response to the Office Action mailed June 6, 2005, Applicant respectfully requests reconsideration.

As a preliminary matter, Applicant has changed the dependency of claim 5 to be dependent on claim 1. Also, Applicant has changed the dependency of claim 11 to be dependent on claim 1. These amendments are for clarification only and not related to any reason for patentability and do not narrow the scope of the claims.

Claim 12 was rejected under 35 U.S.C. §102(b) as being anticipated by Higuchi et al.

Although Applicant respectfully disagrees with this rejection, Applicant has amended claim 12 to additionally recite the step of selectively connecting an incoming data signal from the input stage and a zero signal to the said data input nodes of the register. As this limitation is not taught or suggested by Higuchi, claim 12 distinguishes over Higuchi and withdrawal of the rejection under 35 U.S.C. §102 is respectfully requested.

Accordingly, claim 12 should now be in allowable condition.

Claims 1, and 5-11 were rejected under 35 U.S.C. §103(a) as being unpatentable over Higuchi in view of Erickson et al. Applicant respectfully disagrees with this rejection.

The present application describes performing cyclic redundancy checks (CRC) using a chain of flip-flops, whereby the CRC function is selectable by the user using a multiplexer (MUX) and exclusive-OR (XOR) gate between selected flip-flops, and the length of the CRC polynomial is variably selectable using feedback connections.

Embodiments of the present invention described in the present application differ from Higuchi in the configuration of the circuit elements disposed between the flip-flops. The present application illustrates a configuration in which a first input to an XOR gate is connected to the output of a preceding flip-flop, a second input of the XOR gate is connected to the output of a MUX, and the output of the XOR gate is connected to the input of a following flip-flop. The MUX can selectively pass to its output either a signal from the input stage of the CRC circuit or a zero signal.

Higuchi, on the other hand, illustrates a configuration in which a first input of a MUX is connected to the output of a preceding flip-flop, a second input of the MUX is connected to the

output of an XOR gate, and the output of the MUX is connected to the input of a following flip-flop. The XOR gate has a first input connected to the input stage of the CRC circuit and a second input connected to the output of the preceding flip-flop.

From the perspective of digital logic, these two circuit configurations might appear to perform the same function. However, the configuration illustrated in the present application provides specific technical advantages over that used in Higuchi. Applicant asserts that the technical advantages are not disclosed in either Higuchi or Erickson, and would not have been obvious to the skilled person at the time of the invention.

One technical advantage of the configuration can be appreciated with reference to Figure 4 of the present application. Figure 4 shows the implementation of an error correction circuit to perform CRC error checking based on both 16-bit and 32-bit polynomials. As stated on page 11, line 10-14, "since the 32-bit and 16-bit CRC polynomials to be used have some common terms and other polynomial configurations need not be considered, the minimum number of circuitry components can be identified and only these need to be provided in hardware". In other words specific polynomials are known, and it is desirable for the CRC circuit to switch between these known polynomials. As particular known polynomials are being used, the circuit configuration described above is only required between particular flip-flops. This gives rise to the type of circuit shown in Figure 4 of the present application.

It can be seen with reference to Figure 4 that the two polynomials being used make use of an XOR gate disposed between certain flip-flops (as outlined on page 11, line 29-30). In the example shown in Figure 4, a total of 13 XOR gates are used between flip-flops. However, it can be seen that the circuit in Figure 4 only uses two MUXs. A MUX is a more complex item to construct in hardware than an XOR gate. Therefore, the configuration illustrated in the present application has the advantage that it uses a larger number of smaller and simpler XOR gates, and a smaller number of larger and more complex MUXs. This therefore gives rise to significant savings in terms of chip-area used and complexity, and therefore subsequent savings in costs.

If the circuit configuration illustrated in Higuchi were to be adapted for use with the same two polynomials as used in Figure 4 of the present application, then as many MUXs are required as XOR gates (13 in this example). Therefore, a significantly larger number of MUXs would be

needed if the circuit in Higuchi were to be used, compared to the circuit the present application. Therefore, this makes the implementation of the circuit larger, more complex and hence more costly in Higuchi.

Without the benefit of the teachings described in the present application in connection with these technical advantages, the skilled person would have no motivation to adapt Higuchi as suggested in the Office Action. Higuchi only describes the case where a fully-variable CRC can be used, and does not mention any case where hardware could be saved by only switching between particular known CRC polynomials (in fact Higuchi teaches away from this concept in paragraph [0019]). Therefore, this gives no suggestion that an alternative circuit arrangement could be used that is more efficient from an implementation perspective, according to the advantage described above.

Furthermore, Erickson also makes no mention that the circuit configuration shown in Figure 6 would have the advantage of saving hardware compared to any other equivalent circuit.

Given only the teachings of Higuchi and Erickson and the general knowledge of the skilled person at the time of the invention, the skilled person would not have been motivated to change the layout of the MUX and XOR gates in Higuchi to that in Erickson. The skilled person would have been lead to believe from these teachings that this alternate configuration would perform the same function with no subsequent advantages in terms of chip area or complexity. Therefore the skilled person would not have contemplated modifying Higuchi in view of Erickson as suggested in the Office Action.

Accordingly, the Office Action has not made out a prima facie case of obviousness and therefore claim 1 distinguishes over Higuchi, Erickson, and any combination thereof.

Claims 5-11 depend from claim 1 and are allowable for at least the same reasons.

Accordingly, withdrawal of the rejection under 35 U.S.C. §103(a) is respectfully requested.

CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

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Respectfully submitted,

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